

SYNCHROTRON-RADIATION COMPUTED LAMINOGRAPHY FOR HIGH-RESOLUTION THREE-DIMENSIONAL IMAGING OF FLAT DEVICES

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Synchrotron-radiation computed laminography (SRCL) is developed and implemented as a method for three-dimensional (3d) imaging of regions of interest (ROIs) in laterally extended devices such as sensors, flip-chip devices and other microsystems. It is based on the acquisition of two-dimensional (2d) projections of the device under rotation around an axis which is inclined with respect to the incident x-ray beam by a defined angle $\theta \leq 90^\circ$ [1].

SRCL can be considered as a technique complementary to computed tomography (CT, $\theta = 90^\circ$) preserving the integrity of laterally extended devices since ROIs have not to be extracted (*e.g.* by cutting): for planar substrates which are aligned roughly perpendicular to the rotation axis, the integral x-ray transmission on the 2d detector does not change significantly during device rotation. In comparison to CT, this alleviates the presence of imaging artefacts due to missing information in projections where the integral transmission would tend to zero.

The potential of SRCL for inspection of microelectronic devices is illustrated by the selected example of a flip-chip bonded device in Fig. 1. After bump bonding, the flip-chip solder joints are not accessible by visual inspection. Image (a) shows a 3d rendition of bump bonds. Voids are clearly visible in the interior of the bump bonds. Such voids affect the long-term reliability of the device when it is exposed to heating/cooling cycles, *e.g.* due to device operation. Images (b) to (d) are reconstructed cross-sectional slices showing a number of large voids and smaller voids, the latter predominantly at the interface to the IC's metallisation layers (top part in b). The Pb-rich phase of the solder is well visible in slice (c), furthermore solder splashes near the bump bonds (small satellite spots). Slice (d) highlights a detail of the metallisations and conduction lines on the IC surface towards the bonding/substrate side.

[1] L. Helfen, T. Baumbach, P. Mikulík, D. Kiel, P. Pernot, P. Cloetens and J. Baruchel, *Appl. Phys. Lett.* **86**, 071915 (2005).

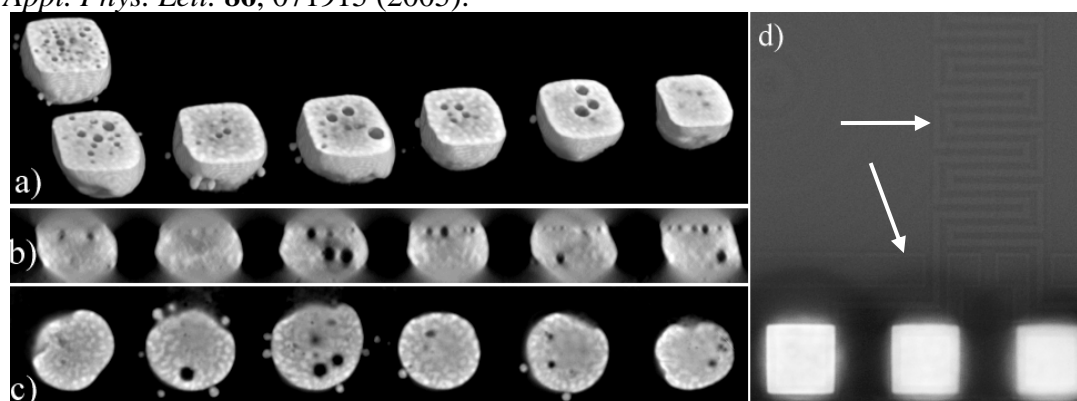


Figure 1. SRCL inspection of a flip-chip bonded device: bump bonds at an IC corner in a 3d rendition (a), two mutually perpendicular slices, perpendicular (b) and parallel (c) to the device surface. Image (d) features a detail of metallisation layers and conduction lines (see arrows) on the hidden surface of the IC. Voxel size is 1.6 μm , x-ray energy range approx. 40 to 60 keV (white beam).

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